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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,457	07/29/2003	Kayoko Shibata	P/126-222	9037

2352 7590 11/04/2004

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EXAMINER	
NGUYEN, DANG T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 11/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,457	SHIBATA ET AL.	
	Examiner	Art Unit	
	Dang T Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-8,10-13, and 15* is/are rejected.

7)☒ Claim(s) *2,9 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to applicant's amendment filed on 08/30/04. Claims 1, 2, 8, 9, 10 and 14 have been amended. Claims 1 – 15 are pending on this application.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3-8, 10-13, and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Funaba et al. U.S. Patent No. 6,411,539 82 - filed Mar. 12, 2001.

Regarding independent claim 1, Funaba et al. discloses a memory module (Fig. 9 [1]) for insertion in any one of connectors (Fig. 9 [104 A –B])) formed on a motherboard (Fig. 11 [MOTHER BOARD]), the module comprising: a memory chip (Fig. 14 [MEMORY CHIPS]; a pin configured and positioned to engage with connector (Fig. 9 disclosing pins are in engaged position with connectors 104A and 104 B); a bus (Fig. 15 [NMOD NBUS]) which connects said memory chip (Fig. 15 [1201]) to said pin; a terminating resistor (Fig. 15 [RESISTOR at 1.25V])

connected to one end of said bus, and a stab resistor (Fig. 15 [RESISTOR between NMOD NBUS and 2101]) connected between said pin and the other end of said bus (Col. 14 lines 24 - 25).

Regarding dependent claim 3, Fig. 11 of Funaba et al. further comprises other memory chips, wherein said bus is connected to all bf the memory chips in common.

Regarding dependent claim 4, Fig. 11 of Funaba et al. further comprising other memory chips, other pins corresponding to said other memory chips respectively, and other buses for connecting said memory chips to said other pins severally.

Regarding dependent claims 5 and 6, even though Funaba et al. are silent to wherein the bus comprises either a bi-directional bus or a unidirectional bus. However the series bus line for memory module taught by Funaba et al. (Fig. 11) must be either a unidirectional or a bi-directional.

Regarding dependent claim 7, Fig. 17 of Funaba et al. discloses wherein said terminating resistor (106) is formed in said memory chip.

Regarding independent claim 8, the claim incorporated substantially samesubject matter as of claim 1, and is rejected along the same rationale.

Regarding dependent claim 10, the claim incorporated substantially samesubject matter as of claim 3, and is rejected along the same rationale.

Regarding dependent claim 11, the claim incorporated substantially same subject matter as of claim 3, and is rejected along the same rationale.

Regarding dependent claims 12 and 13, the claims incorporated substantially same subject matter as of claims 5 and 6 respectively, and are rejected along the same rationale.

Regarding dependent claim 15, the claim incorporated substantially same subject matter as of claim 7, and is rejected along the same rationale.

Allowable Subject Matter

3. Claims 2, 9 and 14 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claims 2 and 9, in addition to other elements in the respective claim, the prior art '539' as applied to claims 1, and 8 above teaches a memory module having a stab resistor connecting between one end of the bus line and the pin, and other end of the bus line is connecting to a terminating resistor. However '539' fails to teach wherein the stab resistance (Rs) and the terminating resistance (Rtem) are given by : Rs = (N - 1) X Zeffdimm/N and Rterm= X Zeffdimm; where N represents the number of said connectors; and Zeffdimm represents effective impedance of a memory chip arrangement podion consisting of said bus and said memory chip.

With respect to claim 14, in addition to other elements in the claim, the prior art '539' as applied to claims 1, and 8 above teaches a memory module having a stab resistor connecting between one end of the bus line and the pin, and other end of the

bus line is connecting to a terminating resistor. However '539' fails to teach wherein the stab resistance (Rs) and the terminating resistance (Rterm) meet an equation of: Zmb = (Rs+ Zeffdimm) /N; where Zmb represents wiring impedance of said motherboard; Zeffdimm represents effective impedance of a memory chip arrangement portion consisting of said bus and said memory chip; and N, the number of said memory modules.

Response to Arguments

5. Applicant's arguments filed 8/30/04 have been fully considered but they are not persuasive.

6. With respect to amended claims 1 and 8, under remarks applicant argued that "Funaba does not teach both the buses and the terminal resistors are not part of the memory modules". Therefore, Funaba does not anticipate the amended claims. Examiner agrees with the Applicant that the reference of Funaba (Fig. 11) shows both the bus and the terminal resistors are on the motherboard, and not part of the memory modules. However, the structural limitation as recited in the independent claims 1 and 8 do not implicitly disclose or teach that the bus and the terminal resistors as a part of the memory module. Note that the 102 rejection is applied to the claim not the specification. Therefore, the argument is not persuasive.

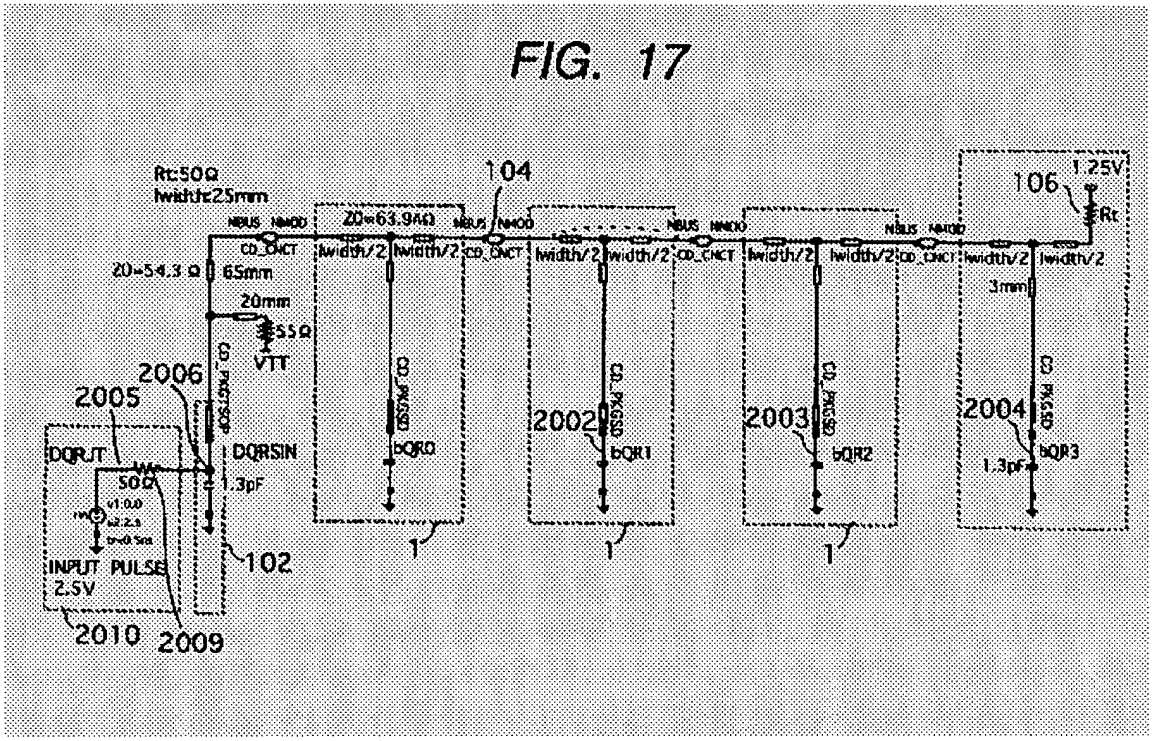

Fig. 17 of Funaba teaches both the buses and the terminal resistors are part of the memory modules.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

8. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen 10/21/2004

RICHARD ELMS
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